ABSTRACT OF THE INVENTION

The invention provides a system and method for memory bus assignment for a plurality of functional devices. According to a preferred embodiment, the invention provides a system comprising a plurality of functional devices accessing a memory bus wherein the memory bus allows access by one of the functional devices for one cycle of period of time, a plurality of request agents corresponding to the functional devices, a control register respectively storing access priority grades for the request agents, a plurality of counter timers respectively loading the access priority grades; and a bus elector coupled with the counter timers wherein the bus elector respectively compares the loaded access priority grades and elects one out of the request agents according to the compared access priority grades. The memory bus accordingly allows access by one of the functional devices corresponding to the elected request agent for one cycle of period of time.